1. Based on the following information about a computer what can be said about its performance?

30% of the instructions are store and execute in 3 clock cycles
10% of the instructions are load and execute in 3 clock cycles
20% of the instructions are ALU register to register instructions that execute in 1 clock cycle.
5% of the instruction are call instructions that execute in 4 clock cycles.
5% of the instruction are return instructions that execute in 6 clock cycles.
30% of the instructions are branch instructions that execute in 2 clock cycles.

The control unit clock operates at 2000 MHz.

(a) 5000 MIPS  
(b) 8000 MIPS  
(c) 400 MIPS  
(d) 800 MIPS  
(e) 1000 MIPS

2. For a computer with cache memory and the following characteristics:

- Physical address space of $2^{64}$ bytes,
- Cache size of $2^{17}$ bytes,
- Set-associative with a set size of 2,
- Cache block size of 64 bytes,

The number of cache blocks in cache is

(a) 64  
(b) $2^{17}$  
(c) 1024  
(d) $2^{11}$  
(e) As many as needed

3. Which of the following properly describe trap software instructions.

(a) Sets the user/supervisor mode status bit.
(b) Causes the sequence of instruction to be trapped.
(c) Is used to transfer control into the operating system.
(d) Is closely related to faults and interrupts.
(e) a, c and d

4. In a computer system with a memory resident stack that is executing a function that may be recursively called, which addressing mode is used to access local variables?

(a) absolute  
(b) register indirect with post increment  
(c) register indirect with displacement  
(d) stack pointer direct  
(e) program counter indirect
5. Of the following statements related to effective address,
   (a) It is a particular location in cache.
   (b) It is related to the instruction addressing mode.
   (c) It can be the sum of a base address and displacement.
   (d) It can be loaded into the program counter.
   (e) It is generated from the set-associative mode.
which are correct?
   (a) a, e
   (b) a, c, d, e
   (c) b, c, d
   (d) a
   (e) all of the above

6. From the following,
   (a) page fault
   (b) saving registers
   (c) locality of reference
   (d) passing parameters
   (e) global addressing
   (f) allocate local variables
   (g) saving return address
which of the above necessarily are performed for the execution (invocation) of functions and procedures?
   (a) a, b, d
   (b) b, c, d, e
   (c) a, c
   (d) b, d, f, g
   (e) c, e, g

7. What is the result of adding 1000 to 0111
   (a) 10000, n=1, z=1, v=1, c=1
   (b) 0000, n=0, z=1, v=0, c=1
   (c) 1111, n=1, z=0, v=0, c=0
   (d) 1000, n=0, z=0, v=1, c=0
   (e) 1111, n=1, z=0, v=1, c=0

8. Which of the following is NOT true about assemble language programming.
   (a) May be used in limited portions of operating systems to increase performance.
   (b) Allows user mode processes to execute in the supervisor mode.
   (c) Makes extensive use of locality of reference.
   (d) Is closely related machine language.
   (e) a and d
9. What is the effective memory speed for a computer with the following memory characteristics:
   • cache speed of 2 nsec.
   • main memory speed of 50 nsec.
   • hit ratio of 95%
   
   (a) 51.9 nsec
   (b) 44.44 nsec
   (c) 6.9 nsec
   (d) 3.4 nsec
   (e) 1.9 nsec

10. Which of the following describes the Ifetch component of the instruction execution cycle.

   (a) \( MAR \to PC \\
       PC \to PC + 1 \\
       MDR \to M[MAR] \\
       IR \to MDR \)

   (b) \( MAR \leftarrow PC \\
       PC \leftarrow PC + 1 \\
       MDR \leftarrow M[MDR] \\
       IR \leftarrow MDR \)

   (c) \( MAR \leftarrow PC \\
       PC \leftarrow PC + 1 \\
       MDR \leftarrow M[MAR] \\
       IR \leftarrow MDR \)

   (d) \( IR \leftarrow PC \\
       PC \leftarrow PC + 1 \\
       MDR \leftarrow M[MAR] \\
       PC \leftarrow MDR \)

   (e) none of the above